**Progress Report**

The main point of checkpoint 4 is competing advanced features on the top of our basic RISC-V project that is supposed to be done by checkpoint 3. This means it includes layers of cache using arbiter system especially separately running Instruction and data cache. Upon the top of this system, we wanted to implement one eviction write buffer in between L2 cache and physical memory along with basic hardware prefetcher and last but not least, mainly a C-extension of RISC-V system. As a progress, we currently have done implemented and merged basic hardware prefetcher. EWB is on debugging stage and C-extension is on our progress still.

**Advanced Features we are trying to implement / had implemented**

~~1) HW based prefetching~~

~~- As of our discussion, we know that this can be done by adding some modules only, such as adding stream buffers, and prefetching signals so it can prefetch data/instruction into stream buffers while execution~~

~~- stream buffer between L1 cache and L2 cache~~

* **Currently implemented and merged with master branch**

2) EWB (single cacheline buffer) paralyzing the WB. Upon a writeback stage, writeback request should be routed to EWB, not our next level of memory, here our physical memory. Then it services the writeback at next available opportunity when the next level cache is free, again for here our physical memory.

- load should only stall if there is a WB performed while EWB is full.

- its in the debugging stage since we have separate caches for instruction and data.

3) RISC-V C extension

**Roadmap (Modified from the last progress report)**

\* Marked with blue color: Modification made from the roadmap of last progress report

04/20: finishing up checkpoint 3 / preparation of upcoming checkpoints

04/21: Begin writing EWB and HW prefetching, share ideas about these along with pipelined cache

04/22: Still working on EWB and basic HW prefetcher / TA meeting

04/23: Merging basic HW Prefetcher in different branch / CP progress report starts

04/24: Debugging basic HW prefetching / CP progress report almost completed

04/25: Debugging / basic HW prefetching is merged / EWB codes are done roughly, discussion continued within the team for EWB and C-extension

04/26: Debugging / Preparation of final report and presentation started

04/27: CP4 due 11:59 P.M / any extra work along with debugging would be done until checkpoint 5 due date which is Wednesday / EWB on debugging and continues on discussion. C-extension is on progress of rough draft of its initial code

04/28: Preparation of final report and presentation continues. If anything is not completed yet, these will be continued along with debugging stages

04:29: Debugging and wrap up the whole MP3 by midnight and prepare for the final presentation.